Organic Electronics 13 (2012) 737–743

Contents lists available at SciVerse ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

One step self-aligned multilayer patterning process for the fabrication of organic complementary circuits in combination with inkjet printing

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ARTICLE INFO

Article history:
Received 24 October 2011
Received in revised form 19 January 2012
Accepted 21 January 2012
Available online 7 February 2012

Keywords:
Polymer circuits
Self-alignment

ABSTRACT

Recent development of solution processable organic semiconductors delineates the emergence of a new generation of air-stable, high performance p- and n-type materials. This makes it indeed possible for printed organic complementary circuits (CMOS) to be used in real applications. The main technical bottleneck for organic CMOS to be adopted as the next generation organic integrated circuit is how to deposit and pattern both p- and n-type semiconductor materials with high resolutions at the same time. It represents a significant technical challenge, especially if it can be done for multiple layers without mask alignment. In this paper, we propose a one-step self-aligned fabrication process which allows the deposition and high resolution patterning of functional layers for both p- and n-channel thin film transistors (TFTs) simultaneously. All the dimensional information of the device components is featured on a single imprinting stamp, and the TFT-channel geometry, electrodes with different work functions, p- and n-type semiconductors and effective gate dimensions can all be accurately defined by one-step imprinting and the subsequent pattern transfer process. As an example, we have demonstrated an organic complementary inverter fabricated by 3D imprinting in combination with inkjet printing and the measured electrical characteristics have validated the feasibility of the novel technique.

1. Introduction

In the development of organic integrated circuits for real application in consumer electronics, improved noise margin (NM) and low power dissipation become more and more critical in addition to the constant need of high device speed [1,2]. A large NM will allow large-scale integration of organic TFTs with an acceptable manufacturing yield while low power dissipation will make the use of organic integrated circuits (ICs) feasible for battery-powered (i.e. portable) applications. The simplest and most effective way to meet these needs is to be able to use CMOS [1], where p- and n-channel TFTs are combined together to construct high-performance circuits with high production yield and excellent power dissipation characteristics [2–4]. There are two key issues to be addressed for the realization of low cost organic CMOS. Firstly it is essential that both p- and n-type semiconductor materials are solution processable, with reasonably high charge mobility, and stable in ambient conditions. Secondly, it is desirable to avoid costly photolithographic based fabrication process in defining the TFT channels, dimension of semiconductors and gate electrodes [5]. Recently, significant progress has been made on developing of p- and n-type solution processable organic semiconductors with high charge mobility and air stability [6,7], and this stimulates the exploration of viable fabrication technology for organic CMOS in terms of manufacturability, yield and fabrication costs.

A range of non-conventional patterning techniques, such as nanoimprint [8], soft-contact-printing [9], micromolding and screen printing [10] have been employed to fabricate organic electronic devices. Whilst these techniques allow

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doi:10.1016/j.orgel.2012.01.019

for patterning with a reasonable resolution, accurate tool alignment with previously defined structures upon the substrate proves to be difficult. This is particularly true for large area and flexible substrates, due to warping and thermal expansion or shrinking of the substrates. In the case of roll-to-roll fabrication, there are further alignment difficulties caused by non-uniform distortions due to the necessary tension applied to the substrate during its movement.

Inkjet printing is a very promising patterning technique in manufacturing of such solution processable electronics [11], in particular for the fabrication of CMOS where both p- and n-type semiconductors need to be deposited [6]. However, the resolution achieved so far by free-format inkjet printing using well developed printers, which rely on either thermal or acoustic formation and ejection of liquid droplets through a nozzle aperture, is still far from that of required by electronic industries. It is limited by the size of the printed liquid droplet and its spreading on the substrate after landing.

There are two main existing approaches to improve the printing resolution. One is to develop new types of inkjet printers/techniques, such as electrohydrodynamic jet printing [12,13], dielectrophoretic printing [14], pyroelectrodynamic shooting [15], charge printing [16], etc. These techniques potentially offer very high resolution, however much efforts are required in further development to avoid/reduce the associated cumbersome aspects, such as high-voltage applied between the liquid reservoir and substrate, limitation of inks (charged liquid or dielectric particles), etc. Another approach is to use surface energy patterns created by lithography techniques to confine the printed liquid, guide the liquid flow by proper functionalized surface of material [17], produce ink receding induced narrow hydrophobic lines [18], or combine inkjet printing with a dip-pen-like dragging process to create small features [19].

Generally, the substrate pre-patterning can only allow one layer, like TFT channel, to be patterned with an enhanced resolution. Many problems which are crucial in order to achieve high density integration, such as deposition and patterning of both p- and n-type semiconductors, electrodes with desired work-function for both p- and n-channel TFTs, remain to be addressed.

After numerous attempts in the past decade, several significant progresses were made in developing self-aligned patterning techniques for printed TFTs. The whole development had taken a number of steps before reaching its current stage, including high resolution patterning in one layer (TFT channel) [20], two layers (both channel and gate) [21,22], and three layers (channel, gate, semiconductor) [23,24] of the TFTs in association with inkjet deposition. The latest challenge is to develop a new method similar or superior to that of 3D-imprinting defined three-layer self-aligned patterning used in the fabrication of silicon TFTs/circuits [25–27] where inkjet deposition is not in use. The process used with silicon cannot be applied directly here, because a four-layer self-aligned process is ideally needed for the organic CMOS circuits to pattern both high and low work-function electrodes in addition to p- and n-type semiconductors. In this work we report a process of fabricating organic CMOS circuitry with high resolution by using a single step self-aligned patterning for four-layers through imprinting in combination with inkjet printing. The imprinting tool in use is designed with a structure of 3-indentation-levels for the definition of the dimensions of different functional layers. The dimensions of the TFT-channel, source/drain electrodes with proper work functions, p- and n-types of semiconductors and effective gate can all be defined simultaneously by a one-step imprinting and then realized in the subsequent pattern transfer processes.

2. Fabrication process

Fig. 1 illustrates our fabrication process for an organic complementary inverter. Two conductive layers are predeposited on a substrate, where one conductive layer has a relatively high work function (such as Au or Pt) and the other layer has a relatively low work function (such as Al or Ti). A polymer resist layer is spin-coated on the conductive layers. Then, a stamp is pushed to imprint the resist under a given temperature (Fig. 1(a)). Subsequently, a plasma etching is applied to etch through the bottom of imprinted trench entirely, followed by a wet (or dry) etching to define the TFT channels in the conductive layers by using the resist as an etching mask (Fig. 1(b)). Plasma etching is applied again to expose one pair of source-drain electrodes, followed by a wet etching to remove the top conductive layer of this pair of electrodes (right side of Fig. 1(c)). Plasma etching is applied once again to expose another pair of electrodes (left side of Fig. 1(d)). Thus, two pairs of electrodes with high and low work functions, respectively, are defined. This is essential for the hole and electron injection into p- and n- channels [28,29], respectively. Both p- and n-type semiconductor materials are deposited by inkjet printing (Fig. 1(e)). To improve the surface energy contrast (phobic-/philic-) between the polymer resist bank and the substrate/electrodes, either a plasma treatment or the deposition of a phobic self-assembled molecule monolayer (SAM) by contact printing can be administrated before the inkjet printing of semiconductor materials. Finally, the fabrication process is completed by the spin-coating of a dielectric layer followed by the inkjet printing of the gate electrodes (Fig. 1(f)).

The dimension of the printed gate can be reduced by applying hydrophobic SAM before the deposition of the gate electrode [21,22]. However, such a process is not recommended here if we can find a suitable bank material and prepare it with a proper thickness – the reason will be explained later. Bank material selection is crucial as it needs to be easy enough to imprint and robust enough to stand up in the subsequent liquid processes. A simple way to resolve this difficulty is to inset a stable polymer layer between the imprinted resist and the conductive layer, while the whole fabrication process remains same (Fig. 2).

In this work, titanium (30 nm) and gold (100 nm) layers are deposited on a glass substrate by sputtering. They are chosen to be the conductive layers because the values of their work functions (Au ~ -5.2 eV, Ti ~ -4.3 eV) which favor hole and electron injections into the p- and n-type semiconductors, respectively [29]. Furthermore, the Ti layer will act as a good adhesion layer for the Au layer. Poly(methyl methacrylate) (PMMA) or polystyrene (PS) is used as the resist for imprinting while polymethylglutari-

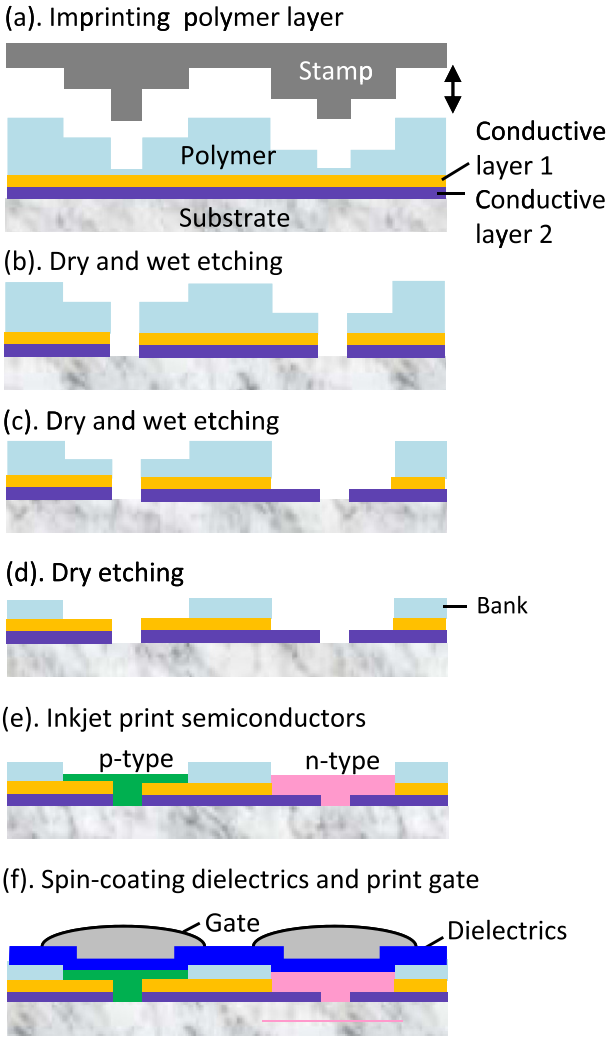

Fig. 1. Schematic illustration of organic CMOS inverter fabrication process using our one-step self-aligned process.

mide (PMGI) is chosen for the inserting polymer layer. The PMMA (or PS) layer has a relatively low glass transition temperature which is favorable for imprinting. While the PMGI layer with a glass transition temperature of 205 °C is thermally stable when the imprinting is carried out. The PMGI banks are robust enough to resist the solvent attacks during the subsequent solution process. A PMGI (900 nm) layer and a PMMA (2.5 μm) are spin-coated in turn on top of the Au/Ti layers and baked at 210 and 100 °C for 10 min, respectively. The PMMA layer is imprinted using a silicon stamp at 160 °C under a pressure of ~50 bar (Fig. 2(a)). After entirely etching through the deep trenches by plasma (O_2 + CF_4 gas mixture) the Au/Ti is etched sequentially in gold etchant (KI:I_2:H_2O = 4:1:200) and 1%HF aqueous solution, respectively, to define the TFT channel using the polymer resist as an etching mask (Fig. 2(b)). Plasma etching is further applied to expose the metal electrodes and a wet etching is followed to remove the top Au layer in order to define the Ti electrodes for n-channel TFTs (Fig. 2(c)). Plasma etching is applied again to expose the Au electrodes for the definition of p-channel TFTs. The remaining PMMA is then removed by acetone and PMGI is left as the banks to confine the printed semiconductor droplets (Fig. 2(d)). Both p- and n-type semiconductor polymers, poly(3,3‴dialkylquaterthiophene) (PQT-12, American Dye Source, Inc.) with HOMO (highest occupied molecular orbital) ~ −5.24 eV [30] and {poly {[*N*,*N*0-bis(2-octyldodecyl)-naphthalene-14,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)}} [P(NDI2OD-T2), Polyera Corp.] with LUMO (lowest unoccupied molecular orbital) ~ −4.0 eV [6] are dissolved in 1,2-dichlorobenzene at 1 wt.% and inkjet deposited, respectively. After baking the printed semiconductors at 110 °C for 4 h in ambient condition, a PMMA dielectric layer of 800 nm in thickness is spin-coated and baked at 90 °C for 30 min. Finally, a poly(3,4-ethylenedioxythiophene):polystyrene (PEDOT:PSS) aqua suspension is inkjet deposited for the gate electrodes. To increase the printing resolution a thin polyvinylphenol (PVP, ~5 nm) is spin-coated on top of the dielectrics before printing the PEDOT:PSS.

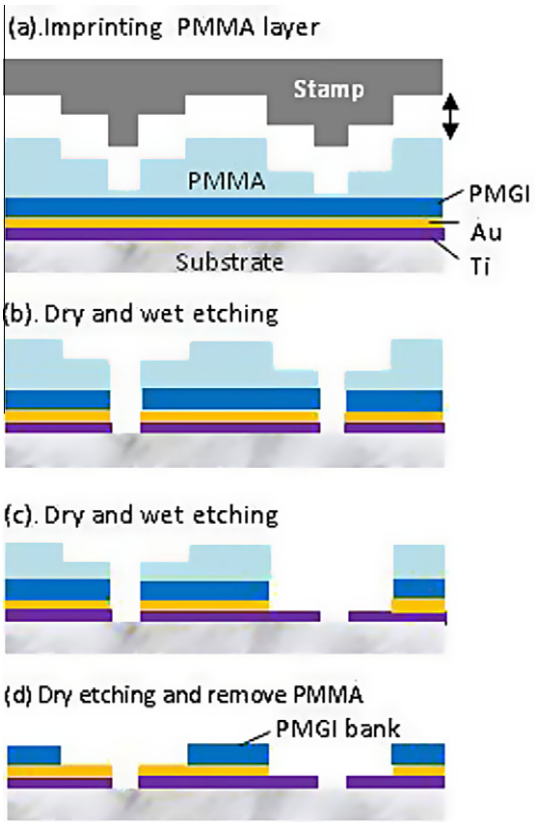

Fig. 2. Schematic illustration of bank fabrication using a thermally stable inserting polymer layer. After bank definition in step (d) the subsequent process is identical with Fig. 1(e) and (f).

3. Result and discussion

Fig. 3 shows a silicon stamp (Fig. 3(a)) with a 3-layered structure prepared by 3-step photolithography and dry etching and its negative copy (Fig. 3(b)) in PMMA to demonstrate the imprinted multi-level structures. Fig. 4(a) shows a typical Au and Ti electrode pairs fabricated by the above described process. Fig. 4(b) and (c) shows a close view of the Au and Ti source/drain electrodes shown in Fig. 4(a). By slightly modifying the stamp shape (Fig. 4(d(i, ii))) and using a similar process one can fabricate circuits with identical (for PMOS or NMOS) or dissimilar source/drain electrode pairs (i.e. source and drain electrodes have different work functions), and the later is applicable to ambipolar transistors/circuits [31], lateral diodes for rectification [32], and light emitting transistors [33]. Fig. 4(e) shows such a dissimilar Au/Ti electrode pair which we have fabricated. Other materials, such as conductive oxides, can also be used. Fig. 4(f) shows indium tin oxide (ITO) source/drain electrodes along with PMGI banks and inkjet printed poly(9,9-dioctylfluorene-alt-bithiophene) (2008P, American Dye Source, Inc.) p-type polymer semiconductor dissolved in mesitylene. The ITO electrodes are defined by wet etching using commercial ITO etchant (Merck Chemical).

The PQT-12 and P(NDI2OD-T2) TFTs and organic complementary inverter are characterized in air using an Agilent 4156C semiconductor parameter analyzer, and the TFT performances are shown in Fig. 5. The charge mobility and current on/off ratio is 1.5×10^{-3} cm^2/V s and 10^4 for PQT-12 (Fig. 5(a) and (b)) and 1×10^{-3} cm^2/V s and 4×10^3 for P(NDI2OD-T2) (Fig. 5(c) and (d)), respectively. The channel length/width of all transistors shown here is 20 μm/1 mm, while the printed semiconductors are confined in 40 μm wide gaps between PMGI banks. The result shows that both p- and n-channel devices are stable against ambient oxygen and moisture exposure and mobile ions (from PEDOT:PSS). The transistor with a PEDOT gate requires high quality dielectrics or stable semiconductors to resist ion attack and stable circuits with PEDOT gates were reported by other groups [34,35]. The TFTs fabricated from 2008P semiconductor is not stable in air due to the ion migration from the PEDOT gate through the dielectrics as assisted by moisture in air, but the device performs well when they are tested in nitrogen (Fig. 5(e) and (f)). Fig. 6 shows the transfer characteristics of a PQT-12/P(NDI2OD-T2) complementary inverter which confirms the capability for a basic logical process of the fabricated CMOS. The process described above is scalable for large integrated circuits. Contact via can also be fabricated during the imprinting and pattern transfer process. A further improving of device/logic gate performance and circuit scaling up is underway.

The dimension of a printed gate can be minimized by tuning the wetability of the dielectric surface, but the same approach is difficult to apply when free-format-printing semiconductor materials due to the delicate interface

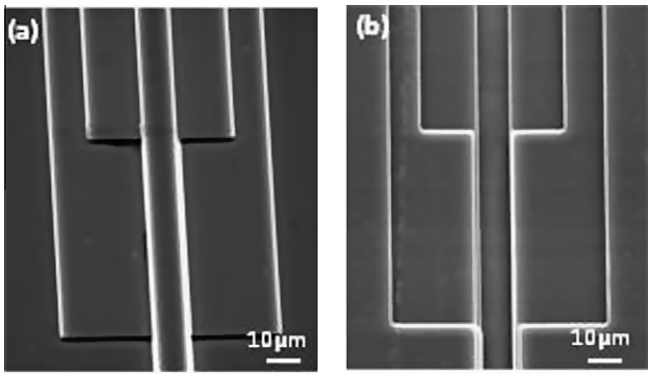

Fig. 3. SEM image of a silicon stamp with structure contrast in three layers (a) and imprinted PMMA structure (b).

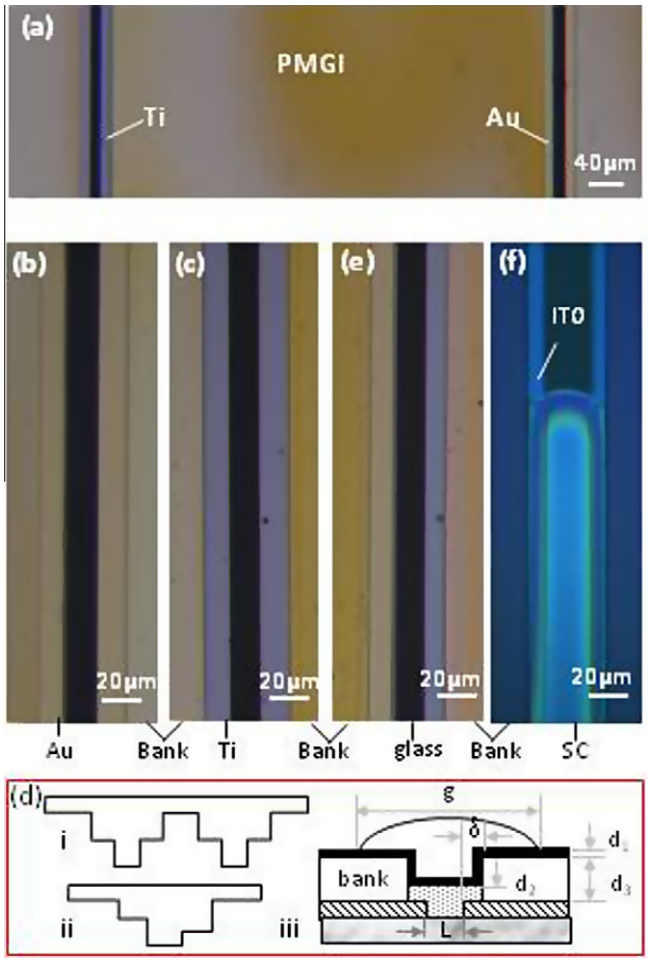

Fig. 4. Photograph of Au and Ti electrode pairs for CMOS inverter (a) and a close view of the Au (b) and Ti (c) source–drain electrodes. (d) Schematic illustration of stamps for PMOS circuits (i) and dissimilar electrodes (ii) fabrication, and a schematic drawing of a TFT with banks (iii). (e) A dissimilar electrode pair with Au and Ti. (f) ITO electrodes and printed polymer semiconductor confined between PMGI banks.

condition between the semiconductor and source/drain electrodes as required by charge injection. The effort for gate dimension reduction is aimed to reduce TFT dimension for high density integration and minimize leakage current and overlapping capacitance between the gate and source/drain electrodes. Since the "self-alignment" of gate is realized by using a 'T' shaped gate, the overlapping capacitance and leakage current can be reduced by using the banks with a proper thickness (of micrometer scale) to effectively separate the gate and source/drain electrodes. As imprint lithography is capable for high resolution patterning, an inter-digital source-drain structure with narrow fingers can be used to further minimize the overlapping capacitance. The width of PEDOT:PSS gate free-format printed by commercial inkjet head can be 30–40 μm without difficulty. This will allow us to fabricate circuits with many thousands of TFTs in 1 cm^2 area which is sufficient for certain applications, such as RFID with multi-bits memory [32]. The ratios of overlapping capacitances (C^*/C) and leakage currants (I_l^*/I_l) between TFTs with and without bank can be estimated as:

$$\frac{C^*}{C} = \frac{2\delta}{g-L} + \frac{\varepsilon_1 d_2 + \varepsilon_2 d_1}{\varepsilon_1 d_3 + \varepsilon_3 d_1}\left(1 - \frac{2\delta}{g-L}\right), \quad (1)$$

$$\frac{I_l^*}{I_l} = \frac{2\delta}{g-L}, \quad (2)$$

where g is the gate dimension (see Fig. 4(d(iii))); L the channel length; δ the length of the exposed source/drain electrodes; $\varepsilon_1(d_1)$, $\varepsilon_2(d_2)$ and $\varepsilon_3(d_3)$ the dielectric constants (thickness) of the dielectrics, semiconductor, and bank material, respectively. Eq. (2) is evaluated by assuming that the bank is thick enough (about or larger than 1 μm) and the leakage current through the bank is negligible. For a typical case, if we take $g \sim 40$ μm, $L \sim 5$ μm, $\delta \sim 0.5$ μm, $\varepsilon_1 \sim 10$, $\varepsilon_2 \sim 6$, $\varepsilon_3 \sim 3$, $d_1 \sim 200$ nm, $d_2 \sim 50$ nm and $d_3 \sim 1$ μm, we can have both C^*/C and $I_l^*/I_l \sim 0.03$, i.e. overlapping capacitance and leakage current will be reduced by 1–2 orders of magnitude and the corresponding operational speed will be increased dramatically.

Here we would like to emphasis the usefulness of the conformal coating of the dielectric layer over the semicon-

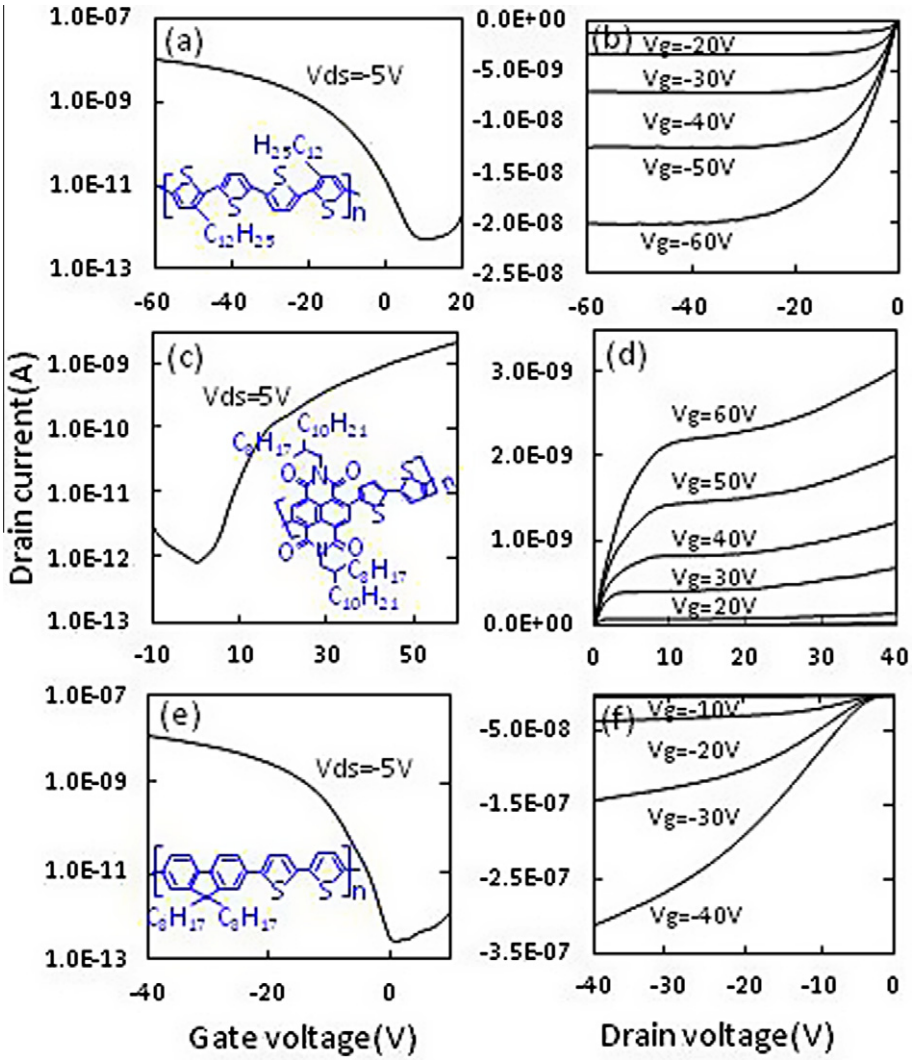

Fig. 5. Transfer (left) and output (right) characteristics of organic complementary TFTs fabricated by the method described in this work (a and b) a TFT with PQT-12 semiconductor and Au electrodes, (c and d) a TFT with P(NDI2OD-T2) semiconductor and Ti electrodes, and (e and f) a TFT with 2008P semiconductor and ITO electrodes.

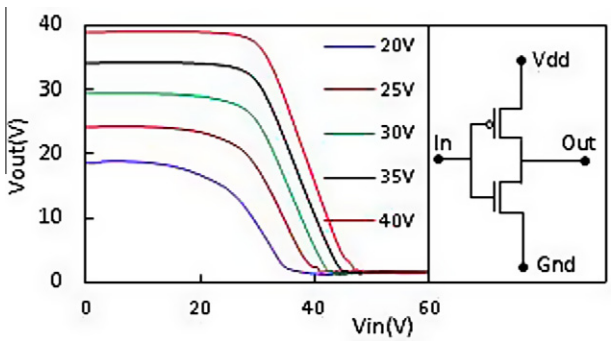

Fig. 6. Output characteristics of an inverter consisting of organic complementary TFTs fabricated by the method described in this work, at various V_{dd} as indicated.

ductors and banks (see Fig. 1(f)). By choosing proper dimensions of the patterned microstructures and the solution used for the coating, the coating layer can be highly uniform and conformal to the coated surface with a layer thicknesses in nanoscale (less than 100 nm) [36]. This is crucial to decrease the driving voltage of the fabricated devices/circuits.

In conclusion, we have proposed a versatile and robust process for the fabrication of organic complementary circuits based on a novel self-aligned multilayer patterning technique in combination with inkjet printing. The dimensions in different functional layers, such as TFT-channel, source/drain electrodes of different work functions, and the geometries of both p- and n-type semiconductor materials and effective gate electrode, can be defined by one-step imprint and subsequent pattern transfer without the need for mask alignment. All the techniques shown here (including imprinting, wet/dry etching, and inkjet printing) are readily available for the fabrications not only on large size planar substrates but also in roll-to-roll configuration. The advantages of high resolution, no mask-alignment, and compatibility to mass production process as shown here illustrate clearly the significant benefit which this technique can bring in when implemented in low cost production of large scale organic complementary circuits.

Acknowledgements

The work was financially supported by Enterprise Ireland (PC/2009/0215). DPC was partly supported by an EPSRC Platform grant.

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